DATA SHEET

M3102A PXIe Digitizers

With Optional Real-Time Sequencing and FPGA Programming 500 MSa/s, 14 Bits, 4 Channels

Improve Your Measurement Fidelity, Signal Integrity and Measurement Throughput

The M3102A are high-performance, high-bandwidth digitizers with an advanced data acquisition system (DAQ). Performance meets simplicity thanks to easy-to-use programming libraries, real-time sequencing technology (Hard Virtual Instrumentation or HVI), and graphical FPGA programming technology.

Features

500 MSa/s simultaneous sampling, 14 bits, 4 channels, 200 MHz BW

Advanced data acquisition system (DAQ)

- Flexible triggering (HW trigger, HVI trigger, SW trigger)
- Programmable cycles and data bursts to avoid PC saturation

Optional HW programming for high-performance applications

- Real-time sequencing (HVI technology)
- FPGA programming
  - Xilinx Kintex-7, 325T or 410T FPGA

Up to 2 GB of onboard RAM (~ 1 Gsamples)

Mechanical/interface

- 1 slot 3U (PXIe)
- PCIe Gen 2
- Independent DMA channels for fast and efficient data transfer

Applications

General purpose digitizer

BB electronics designs and manufacturing in wireless devices

R&D/scientific research equipment

Aerospace & defense (A/D), angle of arrival (AoA)

KEYSIGHT TECHNOLOGIES

Programming Technology and Software Tools

Software programming

- Easy-to-use native programming libraries for most common languages: C, C++, Visual Studio, LabVIEW, MATLAB, Python

Hardware programming (optional)

- Real-time sequencing (Hard Virtual Instrumentation or HVI technology)
  - Graphical flowchart-style M3601A design environment (-HV1 option required on HW)
  - Ultra-fast, fully-parallelized hard real-time execution
  - Ultra-fast, time-deterministic decision-making
  - Off-the-shelf inter-module synchronization & data exchange
- FPGA programming
  - FPGA design environment and BSP support
  - Supports VHDL, Verilog and Xilinx projects, and Xilinx IP Catalog
  - Ultra-fast, one-click compiling and on-the-fly programming

SD1 2.x and SDI 3.x differences

Keysight SD1 2.x software has been upgraded to 3.x. The key differences are listed in the table below. For more detail on SD1 3.x software, refer to the Start Up Guide M3xxx-90002.

[WARNING] The 3.X version of software does not support programs using the M3601A or the M3602A applications. You will have to transition to KS2201A and KF9000A respectively.

SD1 software features	Legacy (SD1 2.1.x)	New (SD1 3.x)
Software		
Design Environment	M3601A HVI design environment (ProcessFlow)	KS2201A PathWave Test Sync Executive (HVI2 technology)
	M3602A FPGA design environment (FPGAFlow)	KF9000A PathWave FPGA Programming Environment (commonly known as PathWave FPGA)
HVI Technology	Graphical M3601A for HV1 HVI-C API (through SD1 installer)	KS2201A PathWave Test Sync Executive (HVI2 Core API through a separate HVI installer)
FPGA Programming	Graphical M3602A PathWave FPGA (BSP for SD1 2.1.x only)	PathWave FPGA (BSP installer for each supported module is required)
Soft Front Panel (SFP)	Available	Available
Programming Interface	Python, C++, C#, LabVIEW, MATLAB	Python, C, C++, C#
Supported Operating System	Windows 10	Windows 10

Hardware Modules		
M3202A (AWG 1G)	FW version<4.0 (CH4) (CLF) (K16, K32, K41) BSP available (K32, K41)	FW version>=4.0 (CH4) (CLF) (K16, K32, K41) BSP available (K32, K41)
M3201A (AWG 500)	FW version<4.0 (CH4) (CLF) (K16, K32, K41) BSP available (K32, K41)	FW version>=4.0 (CH4) (CLF) (K16, K32, K41) BSP available (K32, K41)
M3102A (DIG 500)	FW version<2.0 (CH4) (CLF) (K16, K32, K41) BSP available (K32, K41)	FW version>=2.0 (CH4) (CLF) (K16, K32, K41) BSP available (K32, K41)
M3100A (DIG 100)	FW version<2.0 (CLF) (CH4 or CH8) (K16, K32, K41) BSP available (K32, K41)	FW version>=2.0 (CLF) (CH4) (K32, K41) BSP not available
M3302A (COMBO 500 500)	FW version<4.0 (CLF) (CH2 AWG - CH2 DIG) (K32, K41) BSP available (K32, K41)	FW version>=4.0 (CLF) (CH2 AWG - CH2 DIG) (K41) BSP not available
M3300A (COMBO 500 100)	FW version<4.0 (CLF) (CH2 AWG—CH4 DIG or CH4 AWG—CH8 DIG) (K32, K41) BSP available (K32)	FW version>=4.0 (CLF) (CH2 AWG—CH4 DIG) (K41) BSP not available
No Programming		
Easily configurable SD1 SFP (software front panel) interface for each connected module		

PXIe Arbitrary Waveform Generators, Digitizers and Combination Modules

Product	Type	Outputs (AWGs)				Inputs (Digitizers)			
		Speed (MSa/s)	Bits	Ch	BW (MHz)	Speed (MSa/s)	Bits	Ch	BW (MHz)
M3202A	AWG	1000	14	4	400				
M3201A	AWG	500	16	4	200				
M3102A	Digitizer					500	14	4	DC-200
M3100A	Digitizer					100	14	4/8	DC-100
M3302A	Combo	500	16	2	200	500	14	2	DC-200
M3300A	Combo	500	16	2/4	200	100	14	4/8	DC-100

Note: For SD1 3.x M3100A and M3300A only come in a 4 channel Digitizer version. And M3300A in the 2 channel AWG version.

Ordering Information[1]

Product	Description
M3102A	PXIe digitizer: 500 MSa/s, 14 Bits
M3102A-CH4	Four channels
M3102A-CLF	Fixed sampling clock, low jitter
M3102A-M01 / -M12 / -M20	Memory 16 MB, 8 MSamples / 128 MB, 60 MSamples / 2 GB, 1 GSamples
Software	**License option**
M3601A	HVI design environment
M3602A	FPGA design environment
KS2201A Executive	PathWave Test Sync
KF9000A	PathWave FPGA

1. All options must be selected at time of purchase and are not upgradable
2. These options represent the standard configuration

Functional Block Diagram

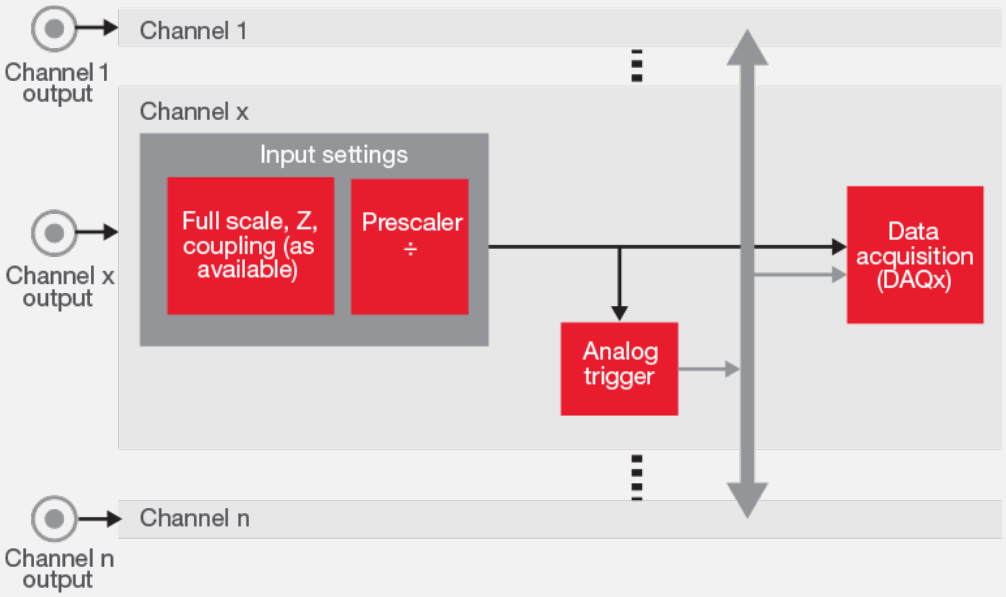


Figure 1. M3102A input functional block diagram, all channels have identical input structure

Technical Specifications and Characteristics

General characteristics

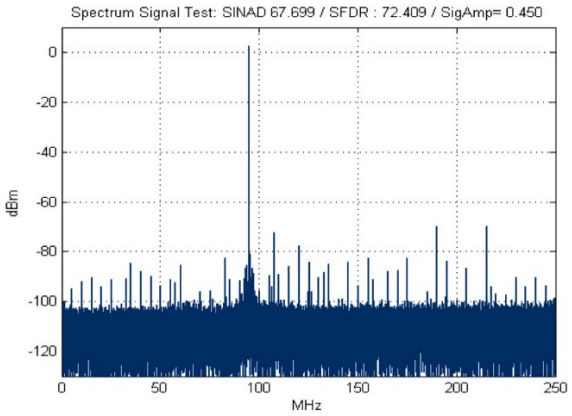
Parameter	M3102A-CH4			Units	Comments
	Min	Typ	Max		
Inputs and outputs					
Channels		4		Out	
Reference clock[1]		1		Out	
Reference clock[2]		1		In	
Triggers/markers[1, 3]		1		In/out	Reconfigurable
Triggers/markers[2, 3]		8		In/out	Reconfigurable
Input channels overview					
Sampling rate		500		MSa/s	
Voltage resolution		14		Bits	
Input frequency	0		200	MHz	
Real-time BW		200		MHz	
Time skew		< 50		ps	Between channels
Built-in functionalities					
Sampling rate		4			1 per channel
Voltage resolution		4			1 per channel
Input frequency		4			1 per channel
Onboard memory					
RAM memory	16		2048	MBytes	

1. At front panel
2. At backplane
3. Markers available from firmware version v3.0 or later

I/O specifications

Analog input characteristics	
Number of channels	CH4
Sampling rate	500 MSa/s
Configurable inputs: Impedance	50Ω or 1MΩ (HiZ)
Configurable inputs: Coupling	AC or DC
Input voltage range (50Ω)	125 mVpp to 8Vpp (7 scales: 0.125, 0.25, 0,5, 1, 2, 4, 8 Vpp)
Input voltage range (HiZ)	200 mVpp to 16Vpp (7 scales: 0.2, 0.4, 0.8, 2, 4, 8, 16 Vpp)
Bandwidth limit filters	200 MHz
Effective number of bits (ENOB)[1]	10.6 bits @ 95 MHz (typical)
Noise floor[1]	-146 dBm/Hz
SINAD[1]	66 dB @ 95 MHz (typical)
Spurious free dynamic range (SFDR) + Total Harmonic Distortion[1]	71 dBc @ 95 MHz (typical)

1. Measured at -1 DBFS input signal with 1 Vpp 50Ω



Parameter	M3102A-CH4 Min	Typ	Max	Units	Comments
Reference clock output					
Frequency		10		MHz	
Voltage		800		mVpp	On a 50Ω load
Power		2		dBm	On a 50Ω load
Source impedance		50		Ω	AC coupled
External I/O trigger/marker					
V_{IH}	2		5	V	
V_{IL}	0		0.8	0.8	
V_{OH}	2.4		3.3	V	On a high Z load
V_{OL}	0		0.25	V	On a high Z load
Input impedance		10		K Ω	
Source impedance		TTL		–	
Speed		100		MHz	

Data acquisition blocks (DAQs) specifications

Parameter	M3102A-CH4 Min	Typ	Max	Units	Comments
General specifications					
DAQs		10			1 per channel
Aggregated speed		800		MSa/s	For all onboard DAQs combined
Acquisition burst multiple		2		Samples	Burst length must be a multiple of this value
Acquisition RAM capacity		50		Samples	Maximum depends on onboard RAM. Number of samples per cycle must be even number
Trigger					Hardware trigger (analog channels, input trigger, backplane triggers), SW/HVI trigger
External I/O trigger/marker					
Speed		500		MSa/s	Per DAQ
Resolution		14		Bits	

Clock system specifications

Parameter	M3102A Min	Typ	Max	Units	Comments
General specifications					
Clock frequency		500		MHz	Fixed clock

System Specifications

Environmental specifications (PXI Express)

Parameter	M3102A-CH4 Min	Typ	Max	Units	Comments
System bus					
Slots		1		Slot	PXI Express (CompactPCI Express compatible)
PCI Express type		Gen 1		–	Automatic gen negotiation, chassis dependent
PCI Express link		1		Lanes	Automatic lane negotiation, chassis dependent
Power dissipation					
3.3V PXIe power supply		1.5		A	~ 5 W
12V PXIe power supply		2		A	~ 24 W

Environmental specifications (PXI Express)

Experimental[1]		
Temperature range	Operating Non-operating	0 to +45°C (10,000 feet) -40 to +70°C (up to 15,000 feet)
Max operative altitude		4000 m (10,000 feet)
Operating Humidity range (%RH)		10 to 95% at 40°C
Non-operating Humidity range (%RH)		5 to 95%
Calibration interval		1 year
EMC		Complies with European EMC Directive – IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A This ISM device is in compliance with Canadian ICES-001 Cet appareil ISM est conforme à la norme NMB-001 du Canada. This ISM device is in compliance with Australian and New Zealand RCM This ISM device is in compliance with South Korea EMC KCC

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

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