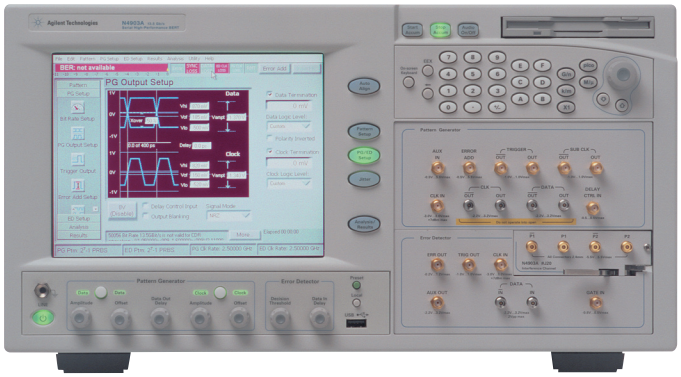
Agilent N4903A High-Performance Serial BERT with complete jitter tolerance testing (J-BERT)

7 Gb/s and 12.5 Gb/s

Data Sheet

Version 1.0



Smartest Characterization

- Calibrated jitter composition
- Integrated into one box
- Automated jitter characterization
- Compliant to latest serial bus standards

New capabilities:

- Integrated and calibrated jitter sources: PJ,SJ, RJ, BUJ, ISI and sinusoidal interference
- Jitter tolerance testing compliant to: PCI Express, SATA, Fibre Channel, FB-DIMM, CEI, 10 GbE, XFP
- Bit recovery mode for analyzing undeterministic patterns
- SSC generation
- Pattern sequencer for generating complex training sequences
- Subrate clock outputs
- Fast total jitter measurement
- All options upgradeable

Agilent Technologies

Agilent Technologies N4900 Series

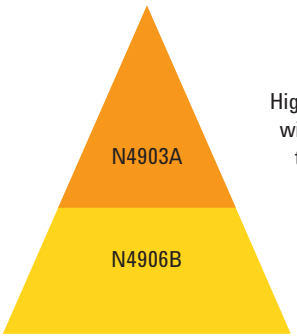
The newest member of Agilent's N4900 Serial BERT series is the powerful N4903A High-Performance Serial BERT (J-BERT). It addresses the needs of R&D and validation teams to characterize serial I/O ports or ASICs up to 12.5 Gb/s. Integrated and calibrated jitter sources for jitter tolerance measurements also allow designers to characterize and prove compliance of their receivers jitter tolerance.

Agilent's N4900 Serial BERT Series is offering key benefits:

- **Excellent precision and sensitivity for accurate measurements**
- **Choice of feature set and frequency classes to tailor to test needs and budget**
- **Pass/Fail testing**
- **State-of-the-art user interface with color touch screen**
- **Remote control via LAN, USB and GBIB interfaces. Compatible with existing command set Agilent 71612, 81630A series, N4900 Series**
- **Small form factor saves rack or bench space**

The N4903A High-Performance Serial BERT is the ideal choice for characterization. It offers fully integrated and calibrated jitter tolerance tests integrated in a high-performance BERT.

The N4906B Serial BERT offers an economic BERT solution for manufacturing and telecom device testing.



Serial BERT applications and selection guide

Device Under Test	Typical Requirements	Recommended Agilent BERT	
		For R&D and characterization	For Manufacturing
Optical Transceivers, i.e.: SONET, SDH, 10GbE, XFP	PRBS Signal precision Eye masks Data rates 10 Gb/s	N4903A	N4906B opt. 012
High-speed serial computer buses, and backplanes, i.e. PCI Express Gen I and II, SATA II and III, SAS, Infiniband-DDR, CEI Fibre Channel 4 G/8 G, etc.	Test pattern sequences CDR Differential inputs Datarates < 7 Gb/s	N4903A*	N4906B opt. 012/101/102
0.6 – 2.5 Gb/s transceiver, i.e. E-PON/ G-PON OLTs, Gigabit Ethernet	Fast bit synchronization Data rates < 3.5 Gb/s	N4906B opt. 003*	N4906B opt. 003

* or ParBERT 81250

Note: options and capabilities that are described in ITALIC are preliminary and not available with first release.

N4903A High-Performance Serial BERT (J-BERT)

The N4903A High-Performance Serial BERT (J-BERT) provides the **only complete jitter tolerance test**. It is the ideal choice for R&D and validation teams characterizing and stressing chips and transceiver modules that have serial I/O ports up to **7 Gb/s or 12.5 Gb/s**. It can characterize a receiver's jitter tolerance and prove its compliance to today's most popular standards, such as **PCI Express, SATA, Fibre Channel, Fully Buffered DIMM, CEI, 10 GbE/XAUI, and XFP**.

Accurate characterization is achieved with clean signals from the pattern generator, which feature exceptionally low jitter and extremely fast transition times. **Test set-up time is reduced** significantly, because the N4903A matches most recent serial bus standards optimally:

- undeterministic patterns can now be analyzed with the **Bit Recovery Mode**.
- A **pattern sequencer** helps to set up training sequences quickly, to get complex devices into loop-back test mode.
- Reference clocks can be provided by the **subrate clock** outputs, which can generate any ratio of clock to data rate.
- All I/Os are **differential** and a **built-in CDR** allows testing of clock-less interfaces.

The N4903A is a **future-proof Serial BERT platform**, which is configurable for today's test and budget requirements but also allows upgrades to all options and full speed.

Available N4903A configurations:

Speed classes, including built-in CDR:

150 Mb/s to 12.5 Gb/s	N4903A-C13
150 Mb/s to 7 Gb/s	N4903A-C07

Jitter Tolerance Options:

RJ, PJ, SJ, BUJ injection	*N4903A-J10*
ISI and Sinusoidal Interference injection	*N4903A-J20*
Upgrade to RJ, SJ, PJ, BUJ	*N4903AU-U10*
Upgrade to 12.5 Gb/s	N4903AU-U13

Pattern Generator Options:

SSC clocking (only in combination with –J10)	*N4903A-J11*

Error Detector Options:

Bit Recovery Mode	*N4903A-A01*

J-BERT key characteristics:

- **150 Mb/s to 7 Gb/s or 12.5 Gb/s – enough margin for characterizing today's most popular serial interfaces**
- **Calibrated and integrated jitter injection (opt. J10). All in one box: RJ, PJ, BUJ, ISI, sinusoidal interference to stress the receiver with >50% eye closure**
- **Automated and compliant Jitter tolerance tests covers popular serial bus standards: PCI Express, SATA, Fibre Channel, SATA, FB-DIMM, CEI 6G/11G, 10GbE/XAUI, XFI/XFP**
- **Delay control input for generator to apply any external jitter source**
- **Bit recovery mode to test unknown data traffic**
- **Pattern sequencer to generate complex training sequences**
- **SSC clocking for computer buses**
- **Subrate clocks to generate reference clocks easily**
- **Differential I/O for DATA and CLOCK and most supplementary signals for testing serial interfaces**
- **Integrated CDR (clock data recovery) to test clock-less interfaces**
- **Highest performance BERT for accurate measurements**
- **All options retrofitable**

Measurements

BER and Measurement suite

- BERT Scan
- Output Timing Jitter
- Spectral Jitter Decomposition
- Eye Contour
- Fast Eye Mask
- Output Level and Q Factor
- Error Location Capture
- Fast Total Jitter

Jitter Tolerance Tests:

- *Manual Jitter Composition (opt. J10)*
- *Automated Jitter Tolerance Characterization (opt. J10)*

Applications

- **PCI Express**
- **SATA**
- **Fibre Channel**
- **Fully Buffered DIMM**
- **CEI**
- **10 GbE**
- **XFP**

Note: options and capabilities that are described in ITALIC are not available with first release.

Jitter Tolerance Tests

Calibrated Jitter Injection:

- *Periodic Jitter (option J10)*
- *Sinusoidal Jitter (option J10)*
- *Random Jitter (option J10)*
- *Bounded Uncorrelated Jitter (option J10)*
- *Intersymbol Interference (ISI) (option J20)*
- *Sinusoidal Interference (option J20)*

External Jitter Injection:
Using an external source connected to delay control input.

User Controls

Manual Jitter Composition (option J10)
of PJ, SJ, RJ, BUJ, ISI and Sinusoidal Interference. This screen allows the user to set up combinations of jitter types and jitter magnitudes easily. Therefore a calibrated 'stressed eye' with more than 50% eye closure can be set up for receiver testing.

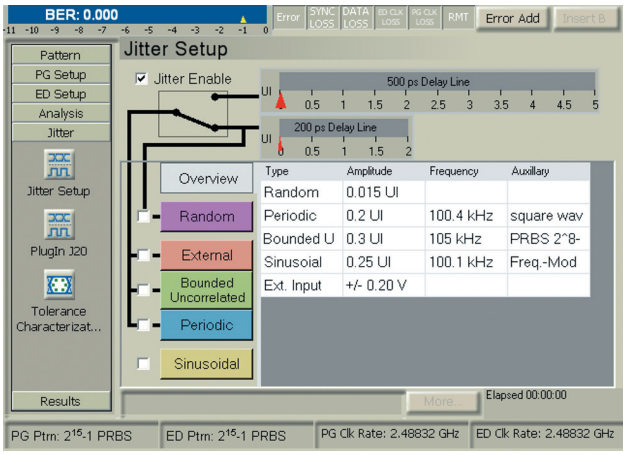


Figure 1: Manual jitter composition (preliminary screen)

Automated Jitter Tolerance Characterization (option J10)
Automated sweep over SJ frequency based on the start/stop frequency, steps, accuracy, BER-level, confidence level and DUT relax time. The green dots indicate where the receiver tolerated the injected jitter. The red dots show where the BER level was exceeded. This automated characterization capability saves significant programming time.

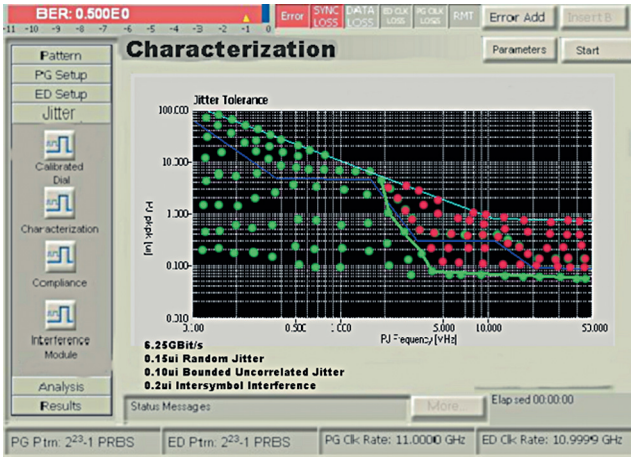


Figure 2: Automated jitter tolerance characterization (preliminary screen)

Note: options and capabilities that are described in ITALIC are not available with first release.

User Interface and Measurement Suite

Spectral Jitter Decomposition

It measures the spectral decomposition of jitter components. The decomposition technique allows the characterization of inband- and outband for circuits and devices including PLLs and CDRs. When debugging designs, the jitter decomposition simplifies identifying deterministic jitter sources.

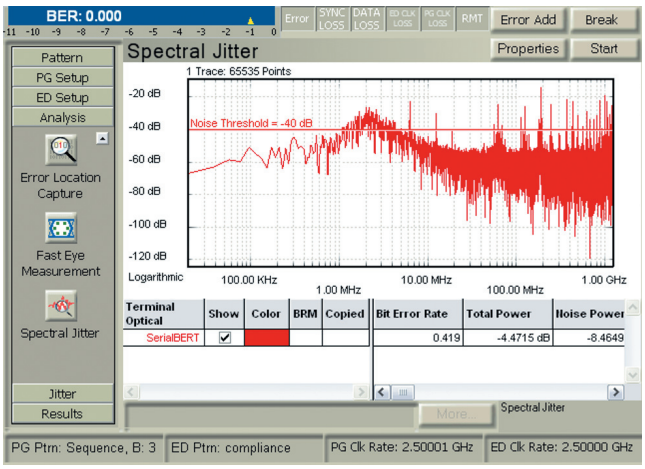


Figure 3: Spectral Jitter Decomposition for debuggung jitter sources in a design

BERT Scan including RJ/DJ separation

This measurement shows the BER versus the sampling point delay, which is displayed as a "bathtub" curve or as histogram. These measurement results are displayed in table of set-up and hold time over phase margin, with total jitter in rms or peak-to-peak, and separated into random and deterministic jitter. The measurement method is equivalent to IEEE 802.3ae.

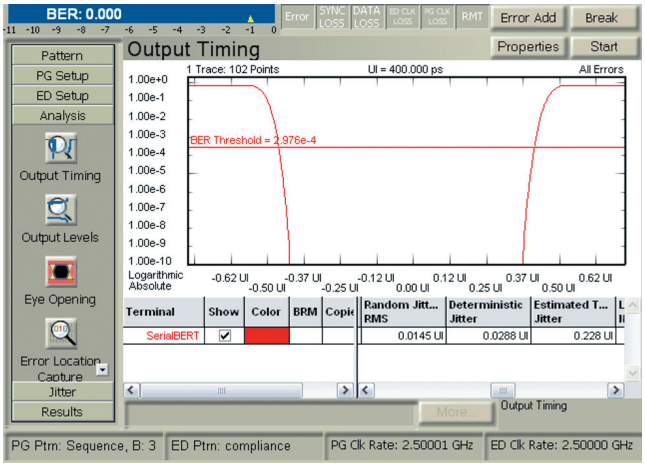


Figure 4: BERT Scan incl. Rj/Dj Separation, Total Jitter

Eye Contour

The eye opening is a key characteristic of a device. The BER is displayed as a function of sampling delay and sampling threshold. Different views are available: Eye Contour (see Figure 5), pseudo colors and equal-BER plots.

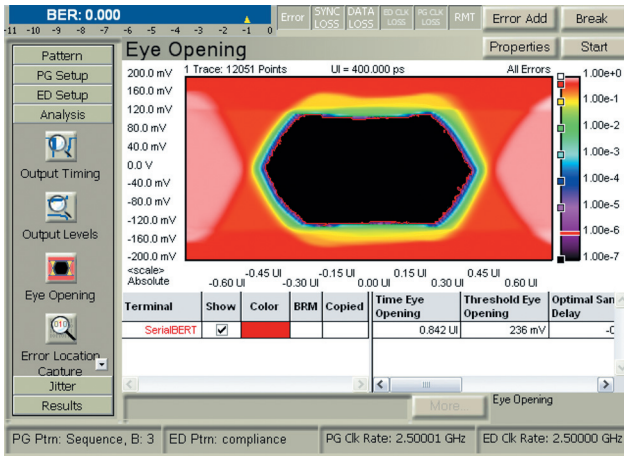


Figure 5: Eye Contour with colors indicating BER-level

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Bit Recovery Mode (option A01)

This mode is useful for analyzing non-deterministic traffic. This is helpful when you need to analyze real-world traffic, for example in a PCI Express link where SKPs are added unpredictably to avoid FIFO overflow. This simplifies set-up by eliminating the need to set up expected data for the error detector. Two analyzer sampling points are used to measure a relative BER, which makes the following measurements possible with relative BER:

- *BERT Scan including RJ/DJ separation*
- *Output levels and Q-factor*
- *Eye contour*
- *Fast eye mask*
- *Fast Total Jitter*
- *Spectral jitter decomposition*

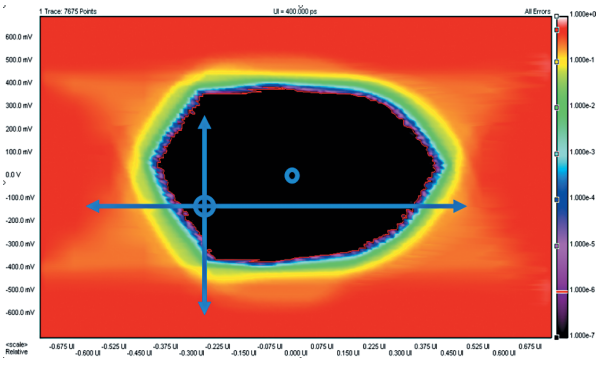


Figure 6: Bit recovery mode for analyzing non-deterministic traffic

Automatic Alignment

The N4903A High-Performance Serial BERT is able to align the voltage threshold and the delay offset of the sampling point automatically, either simultaneously or separately. It is possible to search for the 0/1 threshold automatically on command, and to track the 0/1 threshold continuously.

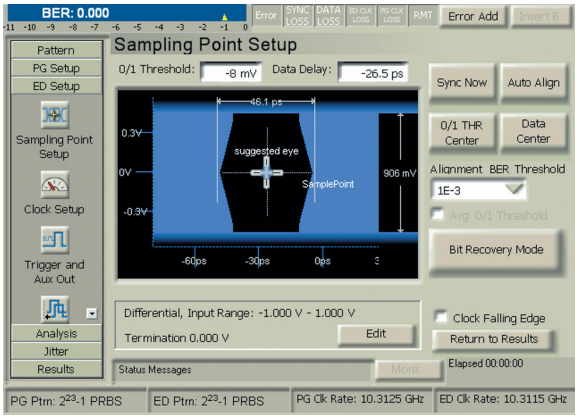


Figure 7: Auto alignment (Center) simplifies correct sampling even for stressed eyes

Fast Total Jitter

Agilent implemented a new measurement technique for TJ (BER), the Fast Total Jitter Measurement. This method provides fast and feasible total jitter measurements, around 40 times faster than a common BERT Scan but with comparable confidence level. Instead of comparing bits until the BER reaches a defined number of bits or a defined number of errors, it only compares bits until it can decide with a 95% confidence level whether the actual BER is above or below the desired BER.

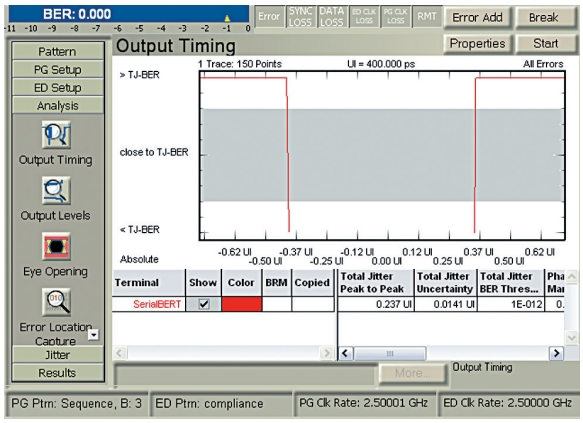


Figure 8: Fast total jitter measurement for quick and accurate total jitter measurements

Note: options and capabilities that are described in ITALIC are preliminary and not available with first release.

Specifications

Pattern Generator Specifications

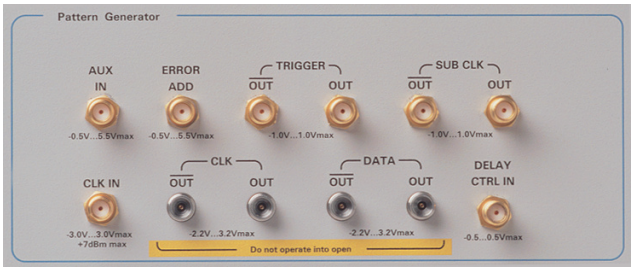


Figure 9: Generator connectors on front panel

Pattern generator key characteristics:

- **Differential outputs for data, clocks and trigger**
- **Variable output voltages covering LVDS, ECL, CML**
- **Transitions times < 20 ps**
- **Clean pulses with Jitter < 9 ps pp**
- **High-precision delay control input to inject jitter from an external source**
- **Calibrated and integrated jitter injection (option J10, J20, both retrofitable)**
- **Subrate clocks for generating any reference clock**
- **Pattern sequencing and 32 Mbit pattern**
- **SSC clocks for computer buses (option J11)**

Data Output (DATA OUT)

Table 1: Output characteristics for N4903A generator. All timing parameters are measured at ECL levels

Range of operation	150 Mb/s to 12.5 Gb/s (opt. C13) 150 Mb/s to 7 Gb/s (opt. C07) < 620 MHz only with external clock. Can be programmed up to 13.5 Gb/s.
Frequency accuracy	± 15 ppm typical
Format	NRZ, normal or inverted
Amplitude/Resolution	0.10 V to 1.8 V, 5 mV steps Adresses LVDS, CML, PECL, ECL (terminated to 1.3 V/ 0 V/-2 V), low voltage CMOS
Output voltage window	– 2.0 V to +3.0 V
Predefined levels	ECL, PECL (3.3 V), LVDS, CML
Transition times [2]	
(20% to 80%)	< 20 ps
(10% to 90%)	< 25 ps
Jitter	≤ 9 ps pp typical
Clock/data delay range	± 0.75 ns in 100 fs steps
External termination voltage [3]	– 2 V to +3 V
Crossing point	Adjustable 20% to 80% typical
Single error inject	Adds single errors on demand
Fixed error inject	Fixed error ratios of 1 error in 10^n bits, n = 3, 4, 5, 6, 7, 8, 9
Interface [1]	Differential or single-ended, DC coupled, 50 Ω
Connector	2.4 mm female

[1] Unused outputs must be terminated with 50 Ω to GND.
[2] At 10 Gb/s and 7 Gb/s
[3] For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.

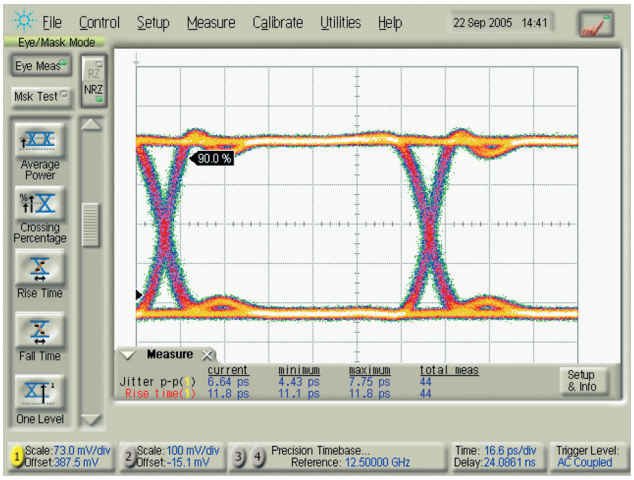


Figure 10: Clean output signal. 10 Gb/s, LVDS levels

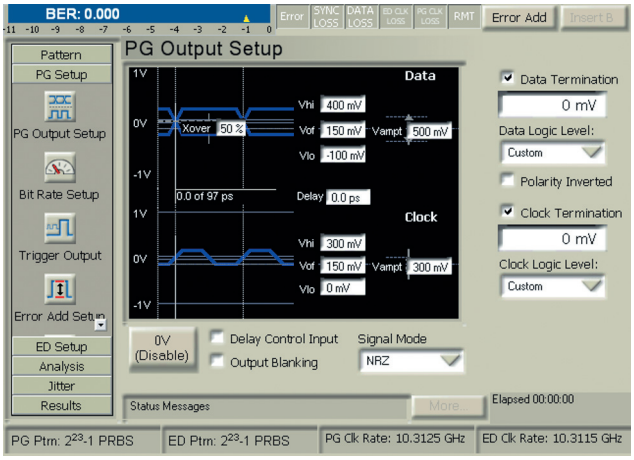


Figure 11: Pattern Generator setup screen

Note: options and capabilities that are described in ITALIC are preliminary and not available with first release.

Clock Output (CLK OUT)

Table 2: Clock output characteristics. All timing parameters are measured at ECL levels

Frequency range	150 MHz to 12.5 GHz (opt. C13) 150 MHz to 7 GHz (opt. C07) <620 MHz only with external clock
Amplitude/Resolution	0.1 V pp to 1.8 V pp, 5 mV steps
Output voltage window	–2.00 to +2.8 V
Transition times [2]	
(20% to 80%)	< 20 ps
(10% to 90%)	< 25 ps
External termination voltage [3]	–2 V to +3 V
Jitter	1 ps rms typical
SSB phase noise	< –75 dBc with internal clock source. 10 GHz @ 10 kHz offset, 1 Hz bandwidth
Interface [1]	Differential or single-ended, DC coupled, 50 Ω output impedance
Connector	2.4 mm female

[1] Unused outputs must be terminated with 50 Ω to GND.
[2] At 10 Gb/s and 7 Gb/s
[3] For positive termination voltage or termination to GND, exter nal termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.

Clock Input (CLK IN) and 10 MHz Reference Input (10 MHZ REF IN)

Clock input: uses an external clock as generator clock.
10 MHz Reference input: If a 10 MHz reference clock is applied, the internal PLL (used to generate the internal clock for the generator) is locked to the applied signal.

Table 3: Specifications for clock input and 10 MHz reference input

Amplitude	200 mV to 2 V
Interface	AC coupled, 50 Ω nominal
Connectors	Clock input: SMA female, front panel 10 MHz Reference Input: BNC, rear panel

Delay Control Input (DELAY CTRL IN)

The external signal applied to delay control input, varies the delay between Data Output to Clock Output. This can be used to generate jittered signals to stress the device under test in addition to the calibrated jitter infection from N4903A.

Table 4: Specifications for delay control input

Range	–100 ps to +100 ps
Sensitivity	400 ps/V typical
Linearity	± 5 % typical
3 dB Modulation Bandwidth	>1 GHz at 10.8 Gb/s data rate
Levels	–250 mV to +250 mV
Interface	DC coupled, 50 Ω nominal
Connector	SMA female

Error Add Input (ERROR ADD)

The external error add input adds a single error to the data output for each rising edge at the input.

Table 5: Specifications for error inject input

Levels	TTL compatible
Interface	DC coupled, 50 Ω nominal
Connector	SMA female

Subrate Clock Output (SUB CLK OUT)

The subrate clock output is used to generate reference clocks, which are subrates of the data rate, for example, a 100 MHz clock for 2.5 or 5 Gb/s PCI Express data rate.

Table 6: Specifications for subrate clock output

Divider factors	n = 2,3...128
Levels	High: + 0.5 V Low: – 0.5 V typical
Transition times	35 ps typical
Interface	DC coupled, 50 Ω, differential or single-ended
Connector	SMA female

10 MHz Reference Output (10 MHZ REF OUT)

Table 7: Specifications for the 10 MHz reference output

Amplitude	1 V into 50 Ω typical
Interface	AC coupled, 50 Ω output impedance
Connector	BNC, rear panel

Note: options and capabilities that are described in ITALIC are preliminary and not available with first release.

Trigger Outputs (TRIGGER OUT)

This provide a trigger signal synchronous with the pattern, for use with an oscilloscope or other test equipment. Typically there is a delay of 32 ns between trigger and data output for data rates ≥ 620 Mb/s. The trigger output has two modes.
Pattern trigger mode: for PRBS patterns; the pulse is synchronized with a user specified trigger pattern. One pulse is generated for every 4th PRBS pattern.
Divided clock mode: the trigger is a square wave with the frequency of the clock rate divided by 2, 4, 8, 10, 16, 20, 32, 64, and 128.

Table 8: Specifications for trigger output

Pulse width	Square wave
Transition times	35 ps typical
Levels	High: +0.5 V; Low –0.5 V typ
Interface	DC coupled, 50 Ω nominal, single ended or differential
Connector	SMA female

AUX Input (AUX IN)

When the alternate pattern mode is activated, the memory is split into two parts, and the user can define a pattern for each part. Depending on the operating mode of the auxiliary input, the user can switch the active pattern in real-time by applying a pulse (Mode 1) or a logical state (Mode 2) to the auxiliary input. If the alternate pattern mode is not activated, the user can suppress the data on the data output by applying a logical high to the auxiliary input (Mode 3).

Table 9: Specifications for auxiliary input

Levels	TTL compatible
Interface	DC coupled, 50 Ω nominal
Connector	SMA female

SSC – Spread Spectrum Clocking (option –J11)

The built-in SSC clock modulation source is available only in combination with option J10.
It generates a frequency modulated clock signal as used in some computer storage standards to spread EMI. If spread spectrum clocking is enabled, sinusoidal jitter is disabled, however all other jitter sources can be used.

Table 10: Spread spectrum clocking (SSC) characteristics

Frequency deviation	*0 to –0.5%, 10% typical accuracy*
Modulation Frequency	*28 kHz to 34 kHz*
Waveform	*Triangle*
Signals impacted	*Always: subrate clock output, data output. User selectable: clock output, trigger output*

Patterns

PRBS: 2^n-1 with n = 7, 10, 11, 15, 23, 31, and 2^n with n = 7, 10, 13, 15, 23, 31.
User-definable pattern: 32 Mbit, independent for pattern generator and error detector.

Generator Pattern Sequencing

The generators pattern sequences can be started on command or by a signal applied to the auxiliary input.
Number of blocks: up to 4; the block resolution of user definable pattern is 512 bits.
Loops: over 4 or fewer blocks. 1 loop level. Loop counter and infinite.

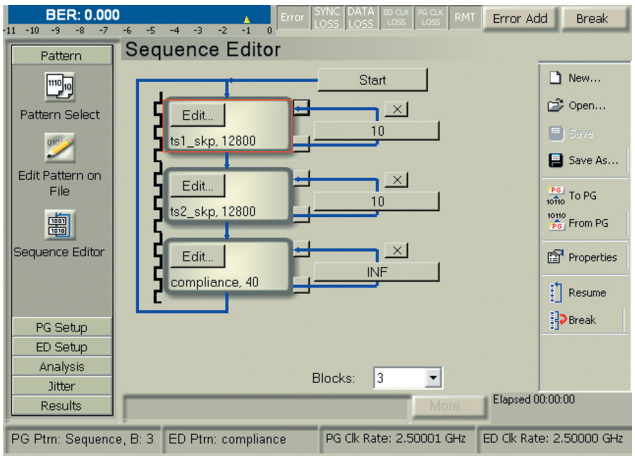


Figure 12: Pattern generator sequencer helps to set up complex training sequences

Alternate Pattern

This allows switching between two patterns of equal length that have been programmed by the user, each of which can be up to 16 Mbit. Switching is possible using a front panel key, over GPIB or by applying the appropriate signal to the auxiliary input port. Changeover occurs at the end of the pattern. The length of the alternating patterns should be a multiple of 512 bits. Two methods of controlling pattern changeover are available: one-shot and alternate.

Zero substitution

Zeros can be substituted for data to extend the longest run of zeros in the patterns listed below. The longest run can be extended to the pattern length-1. The bit following the substituted zeros is set to 1.

Variable mark density

The ratio of ones to total bits in the predefined patterns listed below can be set to 1/8, 1/4, 1/2, 3/4, or 7/8.

Library of predefined patterns

SONET, SDH, FDDI, Fibre Channel, 10 GbE, K28.5

Note: options and capabilities that are described in ITALIC are preliminary and not available with first release.

Error Detector Specifications

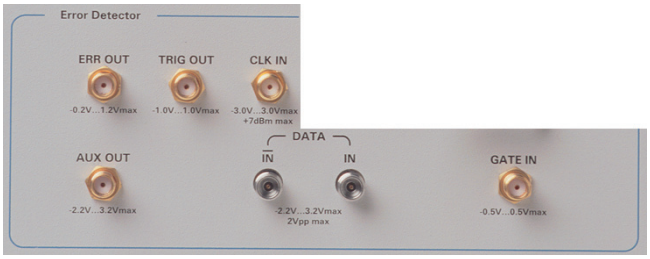


Figure 13: Front panel connectors for error detector

Error detector key characteristics:

- **True differential inputs to match today's ports**
- **Built-in CDR for clock-less data**
- **Auto-alignment of sampling point**
- **Bit Recovery Mode for unknown data traffic**
- **Burst Mode for testing recirculation loop**
- **BER result and Measurement suite**

Data Inputs (DATA IN)

Table 11: Specifications for error detector

Range of operation	150 Mb/s to 12.5 Gb/s (opt. C13) 150 Mb/s to 7 Gb/s (opt. C07)
Format	NRZ
Maximum input amplitude	2.0 V
Termination voltage [1]	–2 V to +3 V or off (true differential mode)
Sensitivity [2]	< 50 mV pp
Intrinsic transition time [4]	27 ps typical 10% to 90%, single ended
Decision threshold range	–2 V to +3 V in 1 mV steps
Maximum levels	–2.2 V to +3.2 V
Phase margin [3]	1 UI – 12 ps typical
Clock/Data sampling delay	± 0.75 ns in 100 fs steps
Interface	Single-ended: 50 Ω nominal, Differential: 100 Ω nominal
Connector	2.4 mm female

[1] Selectable 2 V operating voltage window, which is in the range between –2.0 V to +3.0 V. The data signals, termination voltage and decision threshold have to be within this voltage window.
[2] At 10 Gb/s, BER 10^{-12}, PRBS 2^{31}-1.
[3] Based on the internal clock.
[4] At connector, CECL

Clock Inputs (CLK IN)

The error detector requires an external clock signal to sample data or it can recover the clock from the data signal using the built-in clock data recovery (CDR).

Table 12: Specification for the clock input

Frequency range	150 MHz to 12.5 GHz (option C13) 150 MHz to 7 GHz (option C07)
Amplitude	100 mV to 1.2 V
Sampling	Positive or negative clock edge
CDR output jitter	0.01 UI rms typical
Clock data recovery (CDR)	Loop bandwidth[1] typical
9.2 Gb/s to 11.32 Gb/s	8 MHz
4.23 Gb/s to 6.40 Gb/s	4 MHz
2.115 Gb/s to 3.20 Gb/s	2 MHz
1.058 Gb/s to 1.6 Gb/s	1 MHz
Interface	AC coupled, 50 Ω nominal
Connector	SMA female

[1] The CDR works with specified PRBS patterns up to 2^{31}-1. The CDR expects a DC balanced pattern and a transition density of one transition for every second bit on average.

BER Result Display

The N4903A error detector provides:
1. BER
2. Accumulated BER results
   - Accumulated errored 0's and 1's
   - G.821
   - Error-free intervals
   - Accumulated parameters
   - Burst results
3. Eye results

Note: options and capabilities that are described in ITALIC are preliminary and not available with first release.

Trigger Output (TRIG OUT)

Pattern trigger mode
This provides a trigger synchronized with the selected error detector reference pattern. In pattern mode the pulse is synchronized to repetitions of the output pattern. It generates 1 pulse for every 4th PRBS pattern.

Divided clock mode
In divided clock mode, the trigger is a square wave.

Table 13: Specifications for trigger output

Clock divider	4, 8, 16 up to 11 Gb/s 32, 40, 64, 128 up to 12.5 Gb/s
Levels	High: +0.5 V typical Low: – 0.5 V typical
Minimum pulse width	Pattern length x clock period/2 e.g. 10 Gb/s with 1000 bits = 50 ns
Interface	DC coupled, 50 Ω nominal
Connector	SMA female

Error output (ERR OUT)
This provides a signal to indicate received errors. The output is the logical 'OR' of errors in a 128 bit segment of the data.

Table 14: Specifications for error output

Interface format	RZ, active high
Levels	High: 1 V typical Low: 0 V typical
Pulse width	128 clock periods
Interface	DC coupled, 50 Ω nominal
Connector	SMA female

Auxiliary output (AUX OUT)
This output can be used to provide either clock or data signals:
Clock: clock signals from the input or the recovered clock signals in CDR mode.
Data: weighted and sampled data.

Table 15: Specifications for the auxiliary output

Amplitude	600 mV typical
Interface	AC coupled, 50 Ω nominal
Connector	SMA female

Gating Input (GATE IN)
If a logical high is applied to the gating input the analyzer will ignore the incoming bits during a BER measurement. The ignored bit sequence is a multiple of 512 bits. For measuring data in bursts of bits, rather than a continuous stream of bits, a special operating mode is used. This is the burst sync mode. In this case, the signal at the gating input controls the synchronization and the error counting for each burst. This is an important feature for recirculation loop measurements.

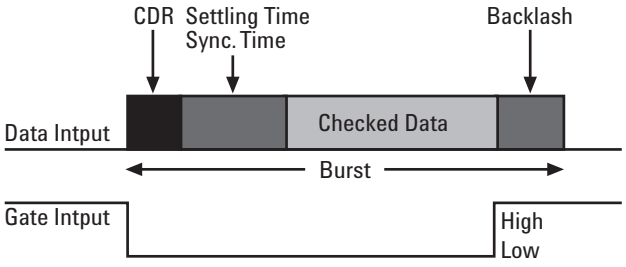


Figure 14: Burst mode allows recirculation loop testing

If clock data recovery (CDR) is used to recover the clock from the burst data, the CDR takes 2 µs from the start of the burst data to settle. The number of bits needed to synchronize itself during a burst depends on whether the pattern consists of hardware based PRBS data or memory based data. To run properly in burst mode the system needs a backlash of data after the gating input returns to high. During each burst, the gating input has to remain passive.

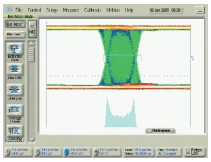
Table 16: Specifications for gating input

Burst synchronization time	1536 bits for PRBS 15 kbit for pattern
Backlash	1536 bits in non-CDR mode 1.5 µs in CDR-mode
Gate passive time	2560 bits in non-CDR mode 2560 bits or 1.5 µs whichever is longer, in CDR-mode
Interface levels	TTL levels
Pulse width	256 clock periods
Connector	SMA female

Note: options and capabilities that are described in ITALIC are preliminary and not available with first release.

Jitter Tolerance Test Specifications

Periodic Jitter (option J10)



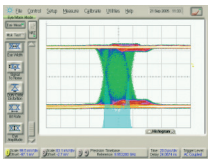
This injects sinusoidal, rectangular or triangular jitter over a wide frequency range.

Table 17: Specifications for periodic jitter (PJ)

Range	*0 to 200 ps pp @ datarates > 3.5 Gb/s* *0 to 500 ps pp @ datarates ≤ 3.5 Gb/s*[1)]
Modulation frequency	*1 kHz to 300 MHz sinusoidal* *1 kHz to 20 MHz triangle* *1 kHz to 20 MHz square wave*
Accuracy	*±10% typical*

1) Available range depends on modulation frequency and data rate.

Sinusoidal Jitter (option J10)



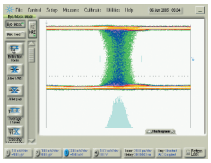
This injects sinusoidal jitter in the lower frequency range with multiple UIs. Covers all high-speed protocols, that is PCI Express, SATA, Fibre Channel, FB-DIMM, CEI 6G/11G, 10 GbE, XFI/XFP.

Table 18: Specifications for sinusoidal jitter (SJ)

Range[1)]	*1000 UI @ 100 Hz* *1 UI @ 4 MHz*
Modulation frequency	*100 Hz to 4 MHz* *(For higher modulation frequencies see Table 17)*
Accuracy	*±10% typical*

1) Available range depends on modulation frequency and data rate.

Random Jitter (option J10)



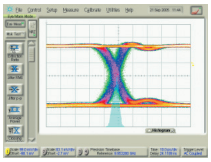
This injects random jitter with a high bandwidth and excellent crest factor.

Table 19: Specifications for random jitter (RJ)

Range	*0 to 14 ps rms* *Crestfactor 14*
Bandwidth	*50 kHz to 1 GHz*
Filter	*10 MHz high-pass,* *500 MHz low-pass.* *Can be turned on/off individually to limit jitter bandwidth.*
Accuracy	*±10% typical*

Note: options and capabilities that are described in ITALIC are preliminary and not available with first release.

Bounded Uncorrelated Jitter (option J10)



This injects a high-probability jitter according to CEI using a PRBS generator and second order low-pass filters.

Table 20: Specifications for bounded uncorrelated jitter (BUJ)

Range	*0 to 200 ps pp @ datarates >3.5 Gb/s* *0 to 500 ps pp @ datarates ≤ 3.5 Gb/s*
PRBS polynomials	*2^n-1; n = 7, 8, 9, 10, 11, 15, 23, 31*
Data rate of PRBS generator	*600 Mb/s to 3.2 Gb/s*
Filters	*20/50/100/200 MHz lowpass 2nd order*
Accuracy	*±10% typical*

Total Jitter

A combination of internally generated PJ, RJ, BUJ and external jitter (injected using external delay control input) is possible:

At data rates > 3.5 Gb/s:

RJ + PJ + BUJ + external delay control input: total delay variation is 200 ps pp max

At data rates ≤3.5 Gb/s:

PJ +BUJ+ external delay control input: total delay variation is 500 ps pp max.

RJ-only: *total delay variation is 200 ps pp max.*

Interference Channel (option J20)

Option J20 is only available in addition to option J10.

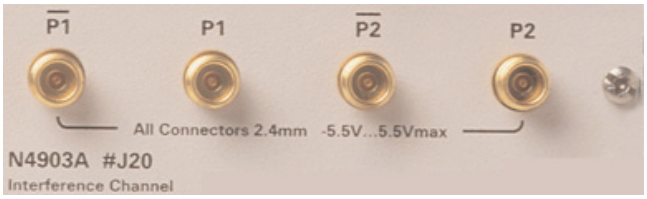
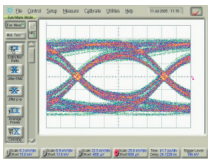


Figure 15: Interference channel connectors

Interference Channel Input and Output (P1, P2)

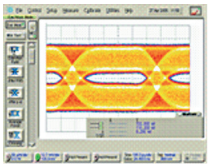


For near-end injection, use P1 as input, for far-end injection, use P2 as input. User selectable board traces are switched into the signal path to emulate a backplane.

Table 21: Specifications for intersymbol interference (ISI)

Trace length	*2, 6, 12, 16, 20, 24, 28, 32, 36, 40 inches of board trace type Nelco 4000-6. When using in combination with sinusoidal interference, minimum trace length is 6 inches.*
S_{21} parameter	*Tbd*
Max. input Levels	*– 5 V to +5 V*
Connectors	*2.4 mm, female*

Sinusoidal Interference (option J20)



This adds common mode, differential or single-ended sine wave signal on top of the data outputs to test common mode rejection of a receiver and to emulate vertical eye closure.

Table 22: Specifications for sinusoidal interference (SI)

Amplitude	0 to 800 mV differential, 0 to 400 mV single ended. *The output signal amplitude is reduced by 3 dB when sinusoidal interference is enabled.*
Frequency	*100 MHz to 3.2 GHz in 100 kHz steps*
Mode	*Common, differential or single ended (on normal or complement) injection*
Level accuracy	*±10% ±10 mV typical*

Note: options and capabilities that are described in ITALIC are preliminary and not available with first release.

Mainframe Characteristics

Table 23: General mainframe characteristics

Operating temperature	5 °C to 40 °C
Storage temperature	– 40 °C to +70 °C
Operating humidity	5° to 40 °C, 95% rel. humidity, non-condensing
Storage humidity	50°C to 70°C, 50% rel. humidity
Power requirements	100 to 240 VA, ±10%, 47 to 63 Hz, 350 VA
Physical dimensions	Width: 424.5 mm Height: 221.5 mm Depth: 580.0 mm
Weight (net) **Weight (shipping) (max)**	26 kg 37.5 kg
Recommended re-calibration period	1 year
Warranty period	1 year return-to-Agilent. See order instructions for extended warranty

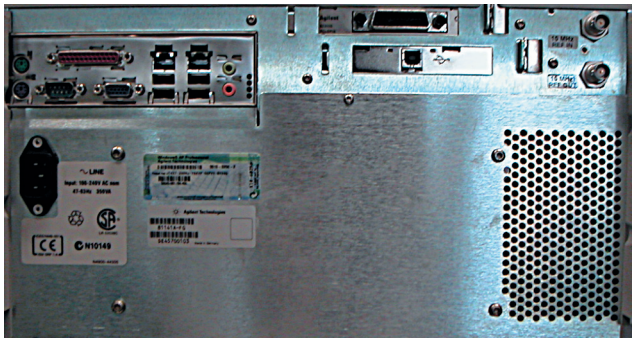


Figure 16: Rear panel view

Display
8" color LCD touch screen

Data Entry
- Color touch screen display, numeric keypad with up/down arrows, dialknob control or external key board and mouse via USB interface
- Pattern export/import

Hard Disk
For local storage of user patterns and data. An external disk is also available for using over the USB interface.

Removable Storage
Floppy Disk Drive 1.44 MB

Remote Control Interfaces
GPIB (IEEE 488), LAN, USB 2.0.
Language: SCPI, *IVI.COM*. SCPI commmands can be exported via copy/paste from the Utility Menu/Output Window

IO Libraries
Agilents IO Libraries suite ships with the N4903A to help quickly establish an error-free connection between your PC and instruments-regardless of the vendor.

Other Interfaces
Parallel printer port, LAN, VGA output, 4 x USB 2.0, 1 x USB 1.1 (front).

Operating System
Microsoft Windows XP

Regulatory Standards
Safety: IEC 61010-1:2001
EN 61010-1:2001
CAN/CSA-C22.2 No.61010-1-04
UL 61010-1:2004
EMC: EN 61326:1997 + A1:1998 + A2:2001
IEC 61326:1997 + A1:1998 + A2:2000
Quality Management: ISO 9004

Specification Assumption
The specifications in this brochure describe the instrument's warranted performance. Non-warranted values are described as typical.
All specifications are valid in a range from 5 °C to 40 °C ambient temperature after a warm-up phase of 30 minutes. If not otherwise stated, all inputs and outputs need to be terminated with 50 Ω to ground. All specifications, if not otherwise stated, are valid using the recommended cable set N4910A (24 mm, 24" matched pair).

Note: options and capabilities that are described in ITALIC are preliminary and not available with first release.

Order Instructions

N4903A High-Performance Serial BERT (J-BERT
Pattern generator & error detector;
5x 50 Ω SMA terminations, 6x adapter SMA female to 2.4 mm male

Speed classes with built-in CDR:

150 Mb/s to 12.5 Gb/s	**N4903A-C13**
150 Mb/s to 7 Gb/s	**N4903A-C07**

Pattern Generator Capabilities:

SSC Generation	***N4903A- J11***
(Only with opt. J10)	

Analyzer Capabilites:

Bit Recovery Mode	***N4903A-A01***

Jitter Tolerance Options:

RJ, PJ, SJ, BUJ Injection	***N4903A- J10***
Interference Channel	***N4903A- J20***

Upgrades:

To 150 Mb/s to 12.5 Gb/s	**N4003AU-U13**
To jitter tolerance-J10	**N4903AU-U10**
(Requires recalibration at Agilent)	

Warranty:

Extended Warranty	**R1280A**

Calibration:

Calibration Services	**R1282A**
Commercial Calibration (N4903A- UK6) with test data is always included	

Productivity Assistance:

Remote or on-site Productivity assistance	**R1380-N49xx** **PS-S20 and PS-S20-02**

Recommended accessories:

2.4 mm cable kit	**N4910A**
Rack mount kit	**N4914A-FG**
47 ps Transition Time Converter	**N4912A**
Adapter 3.5 mm female to 2.4mm male	**N4911A-002**
50 Ω Terminations	**N4912A**

Note: options and capabilities that are described in ITALIC are preliminary and not available with first release.

Related Literature

	Publication Number
N4903A High-Performance Serial BERT Brochure	**5989-3882EN**
Bit Recovery Mode for characterizing idle and framed data traffic Application Note	**5989-3796EN**
N4906B Serial BERT 3 and 12.5 Gb/s Data sheet	**5989-2406EN**
Agilent Physical Layer Test Brochure	**5988-9514EN**
ParBERT 81250 Product Overview	**5968-9188E**
86100 Infiniium DCA-J Data sheet	**5989-0278EN**
Infiniium 80000 Series Oscilloscopes Data sheet	**5989-1487ENUS**
Fast Total Jitter Solution Application Note	**5989-3151EN**
PCI Express 2.0 Testing Application Note	**5989-4087EN**

www.agilent.com/find/N4903

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Printed in the Netherlands, October 13, 2005
5989-2899EN

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